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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 11/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,753	CHU ET AL.	
	Examiner	Art Unit	
	John J Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-17 have been examined.

Drawings

2. Figure 6 is objected to because it is inconsistently labeled with the description in the specification. Page 11, line 16, identifies "a masking register file 52" and Figure 6 identifies a "File Unit 52". A "masking register file 52" is used throughout the specification. Correction for consistency is required.

3. Figure 7 is objected to because it shows the boundary of the "Masking Register File 52" encompassing the "load unit 62" and "feedback loop 68", which is inconsistent with the description in Figure 6 and in the detailed specification, page 13 lines 15-18. Figure 7 should be corrected so the boundary only encloses the latches, and the loading unit is located outside of the masking register file 52.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification describes a "masking register file 52" throughout, however, a "masking register file 52" is not, but a file unit. Correction for consistency is required. This is also to be coordinated with the drawings objection above.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-12, 14, 16, and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

At lines 3-4, the words "having" is vague and word "representing" is wrong of use. It is not clear whether or not the test unit outputs faults in response to a first reference signature.

At lines 7-8, the phrase "the masking unit generating a second reference signature based on the masking data..." is confusing. It is not clear whether the masking unit is connected to the received masking data or the outputted masking data from the loading unit since the loading unit receives the masking data and outputs the masking data (as being recited at lines 5-6).

At lines 11-12, the word "represents" is wrong of use. It is not clear how hardware (a test unit) can represent any fault.

Claim 2-5, 7-11:

Claims 2-5, 7-11 are also rejected because they depend on claim 1 and contain the same problems of indefiniteness.

Claim 6:

At line 2, it is not clear what is being shifted bit-by-bit and what is being matched.

Claim14:

At line 3, it is not clear what is being shifted bit-by-bit.

Claim 16:

The phrase, "feeding back the masking data" in lines 3-4 is unclear. It is not clear where exactly the masking data comes from and where the masking data is fed back to.

Claim 17:

How the latch testing is performed within the masking step in line 4 is unclear.

6. Claim 7 recites the limitation "the output" in line 2, "the file unit" in line 3, "the input" in line 3. There is insufficient antecedent basis for these limitations in the claim.

These limitations are not disclosed in claim 1 in which claim 7 is dependent on. A "file unit" is disclosed in claim 2 not claim 1. It is also unclear whether "the input of the masking unit" refers to masking data or the scanning data (as recited at line 9 in claim 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 9, 11-13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beucler et al. (US-4,779,273) in view of Motika et al. (US-6,516,432 B1).

Claim 1:

Beucler teaches of a register 305 (masking unit) in Fig. 3 that can be loaded with an initial test data pattern. Beucler also teaches the use of a loading unit 301 for the purpose of loading and receiving the test data patterns over a feedback line from the masking unit 301 and inputs it to the array under test 302 (test unit) to save reloading time (col. 4, lines 62-66 and col. 5, lines 5-9). Beucler further teaches (column 2, lines 57-66) of the creation of a new or second reference signature replacing a previous or first reference signature and repeating the process a predetermined number of times. Beucler does not explicitly disclose the method of creating a signature based on masking data and scanning data from a scan string, however, Motika teaches this by the use of a circuit or unit which compares the signature with an expected signature based upon the pattern input to the plurality of scan chain latches, (See col.1, lines 44-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Beucler to add the plurality of scan chain latches as taught in Motika and use that data as a basis of creating a signature with the masking data.

Although Beucler teaches of the creation of a new or second reference signature replacing a previous or first reference signature and repeating the process a

predetermined number of times he does not explicitly disclose the method of running the second reference signature at a new second frequency. Motika, however, suggests the use of a clock control circuit such as an on-product clock generator (OPCG) or a phase-lock-loop (PLL) for modifying clock frequency or timing of the circuit. (See Figure 9, col. 4, lines 41- 44 and col. 7, lines 56-60). The motivation to modify Beucler to use this method of creating a second or new frequency taught by Motika would have been obvious to one of ordinary skill in the art at the time the invention was made. It would have been the motivation of one of ordinary skill in the art at the time the invention was made to add the clock control circuit in Fig. 9 of Motika to automatically control the test frequency.

Claim 12:

Beucler teaches of the creation of a new or second reference signature replacing a previous or first reference signature and repeating the process a predetermined number of times (column 2, lines 57-66). Motika teaches the method of creating a signature based on masking data and scanning data from a scan string by the use of a circuit or unit which compares the target signature with an expected signature, (See col.1, lines 44-46). Motika also discloses a method of identifying a failing pattern when the first reference signature is not equal to the target signature through an AC scan diagnostic method 50 (Fig. 3) that selects a specific failing test pattern sequence and verifies the passing reference point (target signature) and the failing test point conditions (first reference signature). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the method of Beucler in

creating the second reference signature to replace a first reference signature and identify the failing pattern if the first reference signature is not equal to the target signature as taught by Motika. It also, would have been the motivation to one of ordinary skill in the art at the time the invention was made to add the teaching of Motika for identifying a failing pattern to Beucler.

Claim 2, 13 and 16:

Beucler teaches the register (305) for feeding back the signature to the MUX (301). (See col. 4, lines 62-66; col. 5, lines 5-10). Beucler further claims a feedback means for repetitive cycling of the signature through the first routing means for saving reloading time (column 9, line 10 and column 10, line 3).

Claim 3:

Beucler discloses a register 305 (masking unit) in Fig. 3, which is loaded with initial test data patterns. Motika discloses the use of a plurality of shift register latches, which numbers depend upon the width of the input data patterns. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Beucler's register (30) to include the plurality of latches as taught by Motika. Motika teaches also teaches that the number of the latches is not a fixed number and can be modified to any desired number of latches. (See col. 2, lines 50, 55.) It, therefore, would have been obvious to one of ordinary skill in the art at the time the invention was made that the number of latches in Beucler's register (30) can be modified to be equal to or greater than the number in the scan chain on the chip.

Claim 4:

Beucler discloses an array 302 (file unit), for the purpose of receiving masking data from the loading unit MUX 301. Motika teaches the use of a plurality of scan chains for shifting data patterns to create a test signature. Figure 2 discloses the use of scan-only registers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the array in Beucler in view of the teachings of Motika to comprise the file unit of scan-only registers.

Claim 9 and 15:

Beucler teaches of a register 305 (masking unit) in Fig. 3 that can be loaded with an initial test data pattern. Motika further teaches the method of assigning predetermined value to a failing latch for identification purposes in that the two test points and previously identified failing pattern or patterns (masking data) are used to localize the failure to a specific shift register chain, latch, or range of latches. Such localization occurs by modifying the above pattern and timing in conjunction with execution of a search algorithm, such as a binary search algorithm. (See col. 3, lines 46-67 and col. 4, lines 1-44 and Figure 3.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Beucler by assigning a predetermined value to a failing latch by loading the masking unit with the failing pattern and create the signature to localize the failure in view of Motika.

Claim 11:

Beucler teaches a MUX (301) (Fig. 3) for loading and receiving data patterns.

8. Claims 7, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beucler et al.(US-4,779,273) in view of Motika et al. (US-6,516,432 B1) as applied to claim 1 above, and further in view of Nakao et al. (US-2002/0073373 A1)

Claim 7:

Beucler teaches of a compression unit 304 connected to the input of the register 305 (masking unit) that passes a signature. Nakao teaches the use of an OR gate 673 (control unit) connected between the output of storage elements or flip-flops (file unit) and an AND gate 665 (masking unit) for the purpose of controlling the signature on the output of the masking unit with one input of the control unit being an override signal. (See Fig. 13, page 6, paragraph 89). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the compression unit 304 of Beucler to incorporate the function of the OR gate in Nakao to further control the signature at the input of the making unit 665. The motivation would be to withhold the masking data from the making unit, therefore, controlling the data from the file unit 302 in Beucler.

Claim 8:

Nakao teaches the control unit is an OR gate 673. (See Fig. 13, page 6, paragraph 89).

Claim 10:

Beucler teaches of a register 305 (masking unit) in Fig. 3 that can be loaded with an initial test data pattern. Nakao teaches the use of an AND gate 665 for the purpose

of masking data signatures in a test methodology for semiconductors (see Fig. 13, page 6, paragraph 88). It is conventional in testability schemes to incorporate an AND gate in logic design to mask a data pattern based on certain conditions. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the register 305 (masking unit) of Beucler to use an AND gate for the purpose of a masking function taught in Nakao.

9. Claims 5, 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beucler et al.(US-4,779,273) in view of Motika et al(US-6,516,432 B1) as applied to claim 2 and 12 above, and further in view of Koprowski(US-6,021,514).

Claims 5 and 17:

Beucler discloses an array 302 (file unit), for the purpose of receiving masking data from the loading unit MUX 301. Beucler does not explicitly disclose the method for testing a predetermined latch, however, Koprowski teaches the method of forcing selected scan chain latches in the circuit to a predetermined value. Koprowski further discloses that the LBIST design contains logic for generating linehold controls that will apply a specified linehold state to selected scan chain latches during the scan operation portion of the LBIST test. (See col. 2, lines 10-17, 39-42.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the teaching of Koprowski to the teaching of Beucler in order to hold latches within the scan chain to a specified state to select the latches for the exclusive testing.

Claim 6:

Beucler discloses an array 302 (file unit), for the purpose of receiving masking data from the loading unit MUX 301. Motika teaches of loading a plurality of scan chains serially by one or a plurality of scan clocks. Serially loading a scan chain by a scan clock is a bit-by-bit operation. It would have been obvious to one of ordinary skill in the art at the time the invention was made that file unit taught in Beucler should be modified to include a serially loaded scan chain an shifted bit-by-bit as taught by Motika

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beucler et al.(US-4,779,273) in view of Motika et al. (US-6,516,432 B1)and further in view of Kim (US-5,574,733).

Motika teaches the use of a circuit or unit that compares the reference signature with an expected signature based upon the pattern input to the plurality of scan chain latches, (See col.1, lines 44-46). Motika continues to disclose multiple chain test methodologies which include propagating predetermined bit patterns through all scan chains; propagating predetermined sequences through a single chain while all other scan chains propagate a 0; propagating a predetermined pattern through a singe chain while all other scan chains propagate a 1; and/or propagation either of the previous two sequences through multiple scan chains. The examiner asserts, therefore, that the method of shifting data through a scan chain is bit-by-bit by a scan clock (corresponding clock). Kim further teaches a method of performing a built-in self-test on a circuit block

using a reseeding scan chain. The original test seed is first scanned in to the scan chain 391 using test mode. Step 410 is accomplished by asserting one bit of the seed at a time on the scan data in line 380 while applying appropriate clock pulses to the flip-flops 310-318. (See col. 6, lines 35-44.) It would have been obvious to one of ordinary skill in the art at the time the invention was made that data would be shifted through a scan chain bit-by-bit by a clock in view of the teachings of Motika and Kim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J Tabone, Jr. whose telephone number is (703)305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

JJT

CHRISTINE T. TU
Primary Examiner